

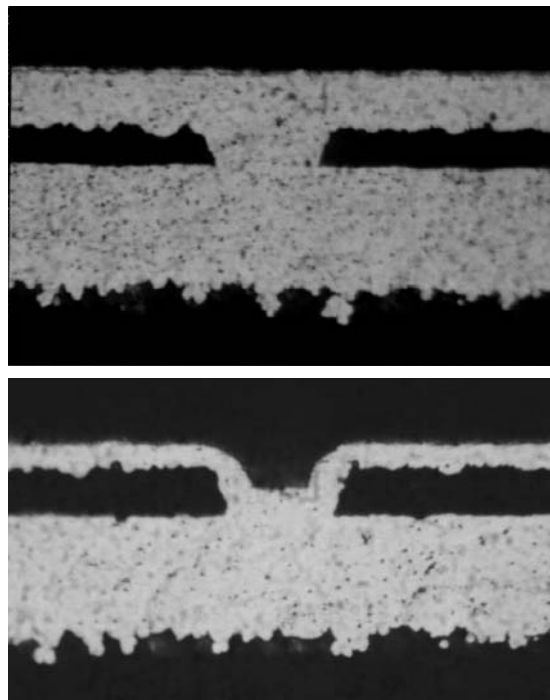
Copper Metallization for VLSI Applications using the *Faradayic* Process

Objective:

This project demonstrated the feasibility of using the patented *Faradayic* Process to deposit copper with minimal overplate, for VLSI features for semiconductor applications.

Summary:

The *Faradayic* Process is used to develop a single step process for copper metallization and planarization 30 μm microvias. The *Faradayic* Process uses a simple, easy to control plating bath consisting of copper sulfate/sulfuric acid and PEG/chloride, only. The Faraday approach fully utilizes the potential of the *Faradayic* Leveling process over a wide range of feature sizes (i.e., submicron-200 μm), to obtain both conformal electrodeposition and trench filling with minimal surface coverage. Since the *Faradayic* Leveling approach consists of an infinite combination of forward, reverse and off-times, it is possible to “tune” the *Faradayic* Leveling waveform for specific applications, provided one understands the nuances associated with the application. Specifically, the current distribution in the microvia applications are governed by microprofile considerations under limited mass transport conditions.



Background:

The patented *Faradayic* Process is an electrochemical manufacturing technique that utilizes a controlled electric field to electrodeposit a material of interest. Since the *Faradayic* Process is electrically mediated, it does not require small amounts of proprietary chemicals to facilitate the metal deposition as needed in conventional electrochemical processes (e.g. DC). The material deposition rate is determined by the applied electric field, which is user-defined and computer controlled. This provides the means for precise control of the length of the process, the total material deposited and the properties of the deposit.

The *Faradayic* Process technology illustrated above is protected by a substantial patent portfolio including issued, allowed, and pending patent actions.