

Non-Contact Polishing for Semiconductor Applications using the FARADAYIC Process

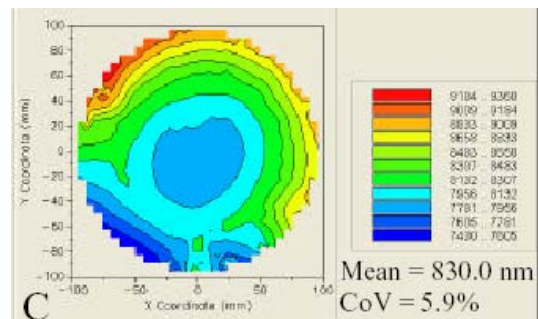
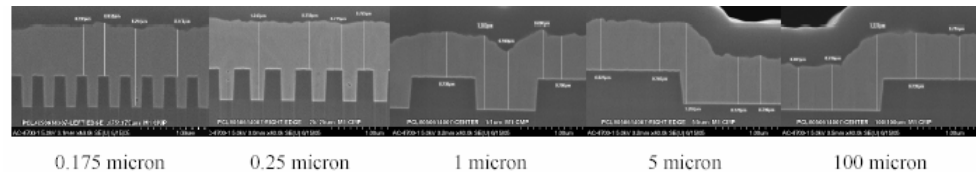
Objective:

This project demonstrated the feasibility of using the patented FARADAYIC Process for non-contact polishing of copper for semiconductor applications.

Summary:

The patented FARADAYIC Non-Contact

Polishing process is a non-contact-stress-free controlled polishing method for planarization of Cu/low- κ interconnects required for the fabrication of nanochip integrated circuits. The FARADAYIC Non-Contact Polishing process utilizes pulsed electrolysis for electrochemical removal of copper overplate, without mechanically stressing the low- κ dielectric substrate. FARADAYIC Non-Contact Polishing utilizes a nonaggressive bath chemistry to enable highly controlled process start and end points, and when used in conjunction with FARADAYIC Electrodeposition produces features without the undesirable momentum bump on semiconductor wafers, and low variation in overplate thickness across the wafer (CoV = 5.9%). Faraday also designed and built a pilot-scale electrochemical cell that can accommodate non-contact polishing of wafer substrates.



Background:

The patented FARADAYIC Process is an electrochemical manufacturing technique that utilizes a controlled electric field for etching, polishing or shaping a metallic work piece. Since the FARADAYIC Process is electrically mediated, it does not require aggressive chemicals to facilitate the metal removal as needed in conventional chemical processes (e.g. chemical etching). The material removal rate is determined by the applied electric field, which is user-defined and computer controlled. This provides the means for precise control of the length of the process and the total material removed. Additionally, the use of neutral salt solutions (e.g. sodium chloride and sodium nitrate) as the electrolyte makes the process both worker and environmentally safe.

The FARADAYIC Process technology illustrated above is protected by a substantial patent portfolio including issued, allowed, and pending patent actions.